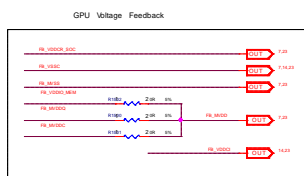


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SHEET NO.	SHEET NAME
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3	Vega10 - GPIO, EXTRA
4	Vega10 - DFTIO, FREE, HPM_DAP, CRACKMON
5	Vega10 - TMDPAB 1xDP, 1xHDMI +5V VESA
6	Vega10 - TMDPEF 2xDP
7	Control - VDDC / MYPD
8	Reg - VDDCR_SOC PHASES I and VII
9	Reg - VDDCR_SOC PHASES V and XI
10	Reg - VDDCR_SOC PHASES III and IX
11	Reg - VDDCR_SOC PHASES IV and X
12	Reg - VDDCR_SOC PHASES II and VIII
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20	THERMAL
21	GPATCH and BACO LEDs
22	DEBUG
23	PI GLUE
24	BLOCK DIAGRAM
25	REVISION HISTORY





//gpuE/doc/design/chip/padding/AI_dGPU/PinStrap_Plan.pptx

TABLE 2		
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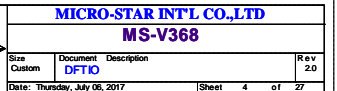
U1T

symbol 20

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AL30	NT CRACKING/DB
Y30	NT CRACKING/DL
Y30	NT CRACKING/DR
Y30	NT CRACKING/DL
Y30	NT CRACKING/DR
BE30	NT CRACKING/DP
BE30	NT CRACKING/DF

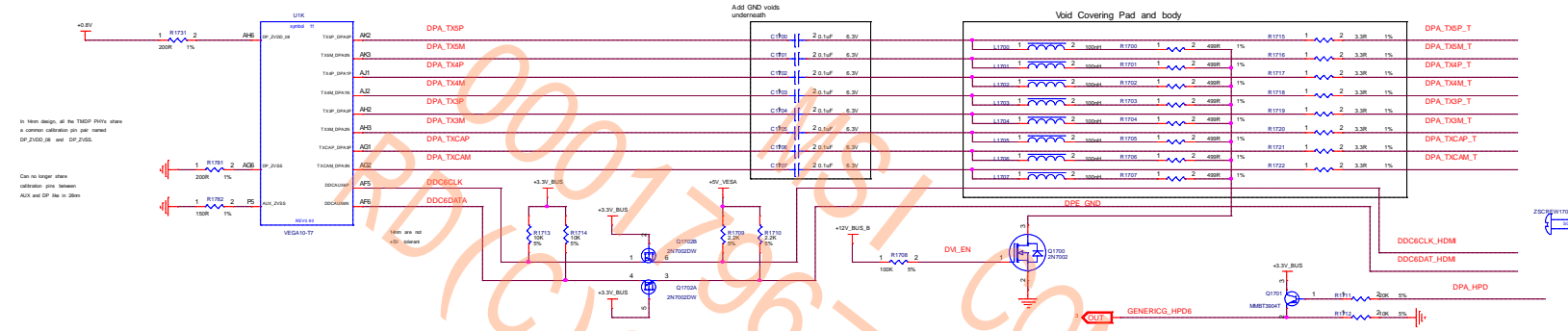
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VEGA10-T7

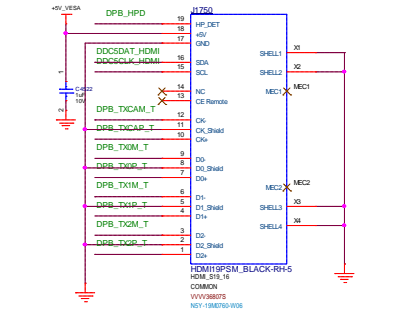
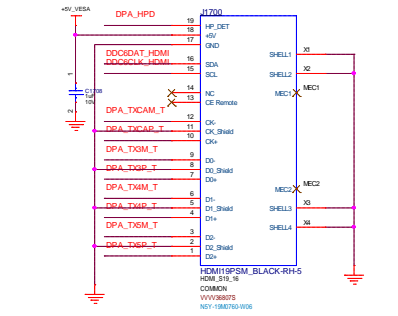
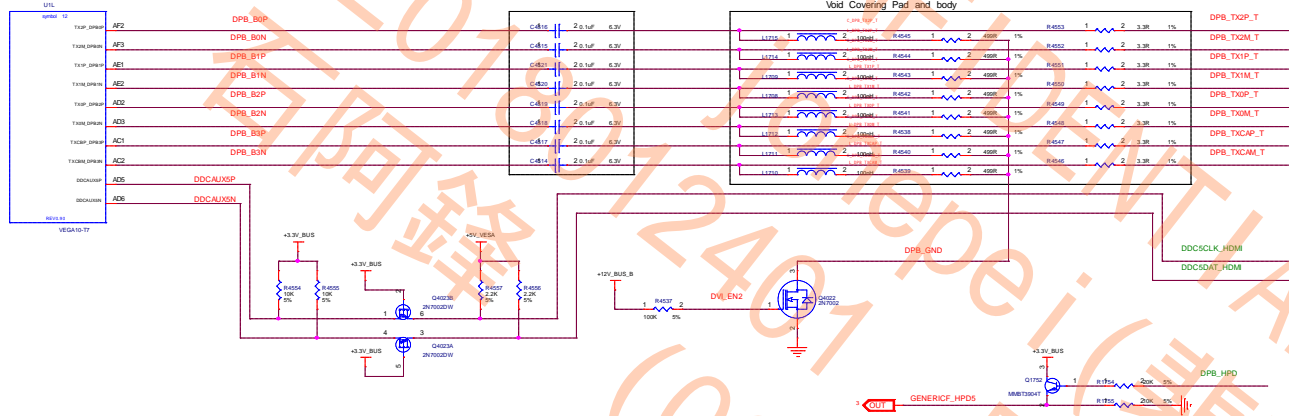


Ensure traces < 5 inches MAX (if routed on same layer)

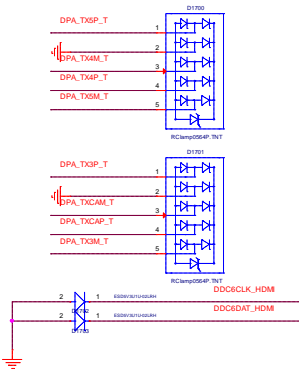
For differential routing on HDMI 2.0 connection, use dogbone shape antipads for the transitional vias of the same differential pair, and the distance from the via edge to the shape boundary should be



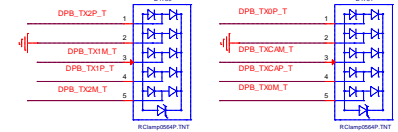
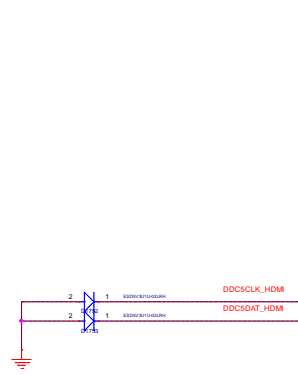
Ensure traces < 5 inches



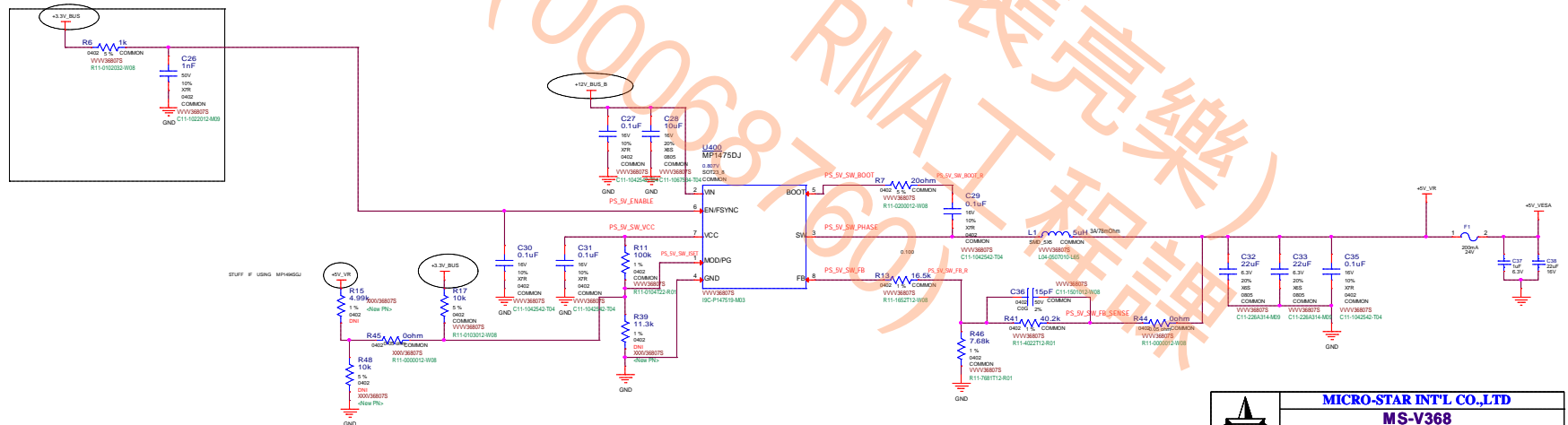
OPTIONAL ESD PROTECTION DIODES



OPTIONAL ESD PROTECTION DIODES

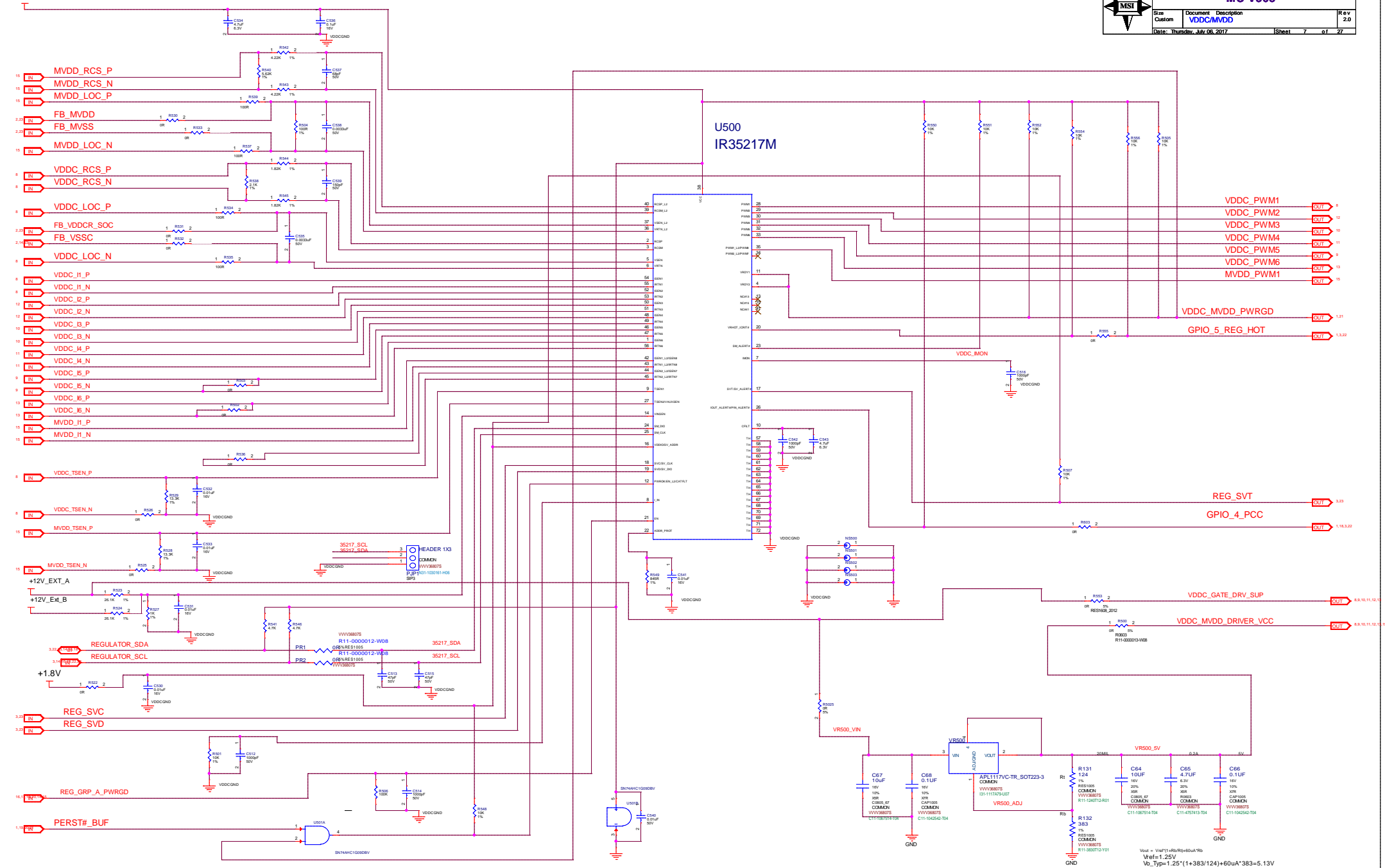


The schematic diagram illustrates the DPE (Digital Power Enable) block and its connections. The block is a large rectangle with multiple pins on the left and right sides. The left side pins are labeled with signals like DPE_E0P, DPE_E0N, DPE_E1P, DPE_E1N, DPE_E2P, DPE_E2N, DPE_E3P, DPE_E3N, DPE_E4P, DPE_E4N, DPE_E5P, DPE_E5N, DPE_E6P, DPE_E6N, DPE_E7P, DPE_E7N, DPE_E8P, DPE_E8N, DPE_E9P, DPE_E9N, DPE_E10P, DPE_E10N, DPE_E11P, DPE_E11N, DPE_E12P, DPE_E12N, DPE_E13P, DPE_E13N, DPE_E14P, DPE_E14N, DPE_E15P, DPE_E15N, DPE_E16P, DPE_E16N, DPE_E17P, DPE_E17N, DPE_E18P, DPE_E18N, DPE_E19P, DPE_E19N, DPE_E20P, DPE_E20N, DPE_E21P, DPE_E21N, DPE_E22P, DPE_E22N, DPE_E23P, DPE_E23N, DPE_E24P, DPE_E24N, DPE_E25P, DPE_E25N, DPE_E26P, DPE_E26N, DPE_E27P, DPE_E27N, DPE_E28P, DPE_E28N, DPE_E29P, DPE_E29N, DPE_E30P, DPE_E30N, DPE_E31P, DPE_E31N, DPE_E32P, DPE_E32N, DPE_E33P, DPE_E33N, DPE_E34P, DPE_E34N, DPE_E35P, DPE_E35N, DPE_E36P, DPE_E36N, DPE_E37P, DPE_E37N, DPE_E38P, DPE_E38N, DPE_E39P, DPE_E39N, DPE_E40P, DPE_E40N, DPE_E41P, DPE_E41N, DPE_E42P, DPE_E42N, DPE_E43P, DPE_E43N, DPE_E44P, DPE_E44N, DPE_E45P, DPE_E45N, DPE_E46P, DPE_E46N, DPE_E47P, DPE_E47N, DPE_E48P, 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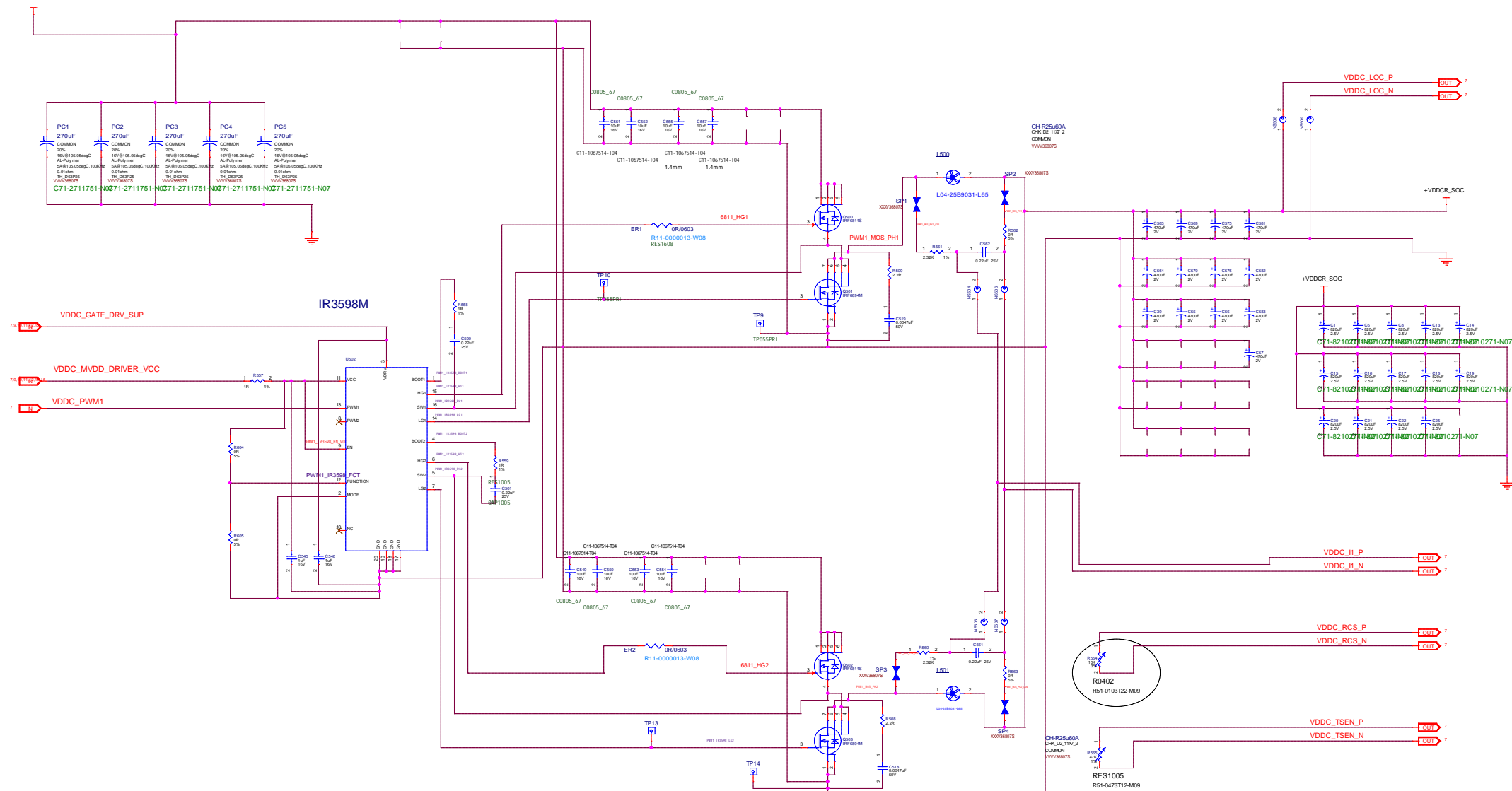


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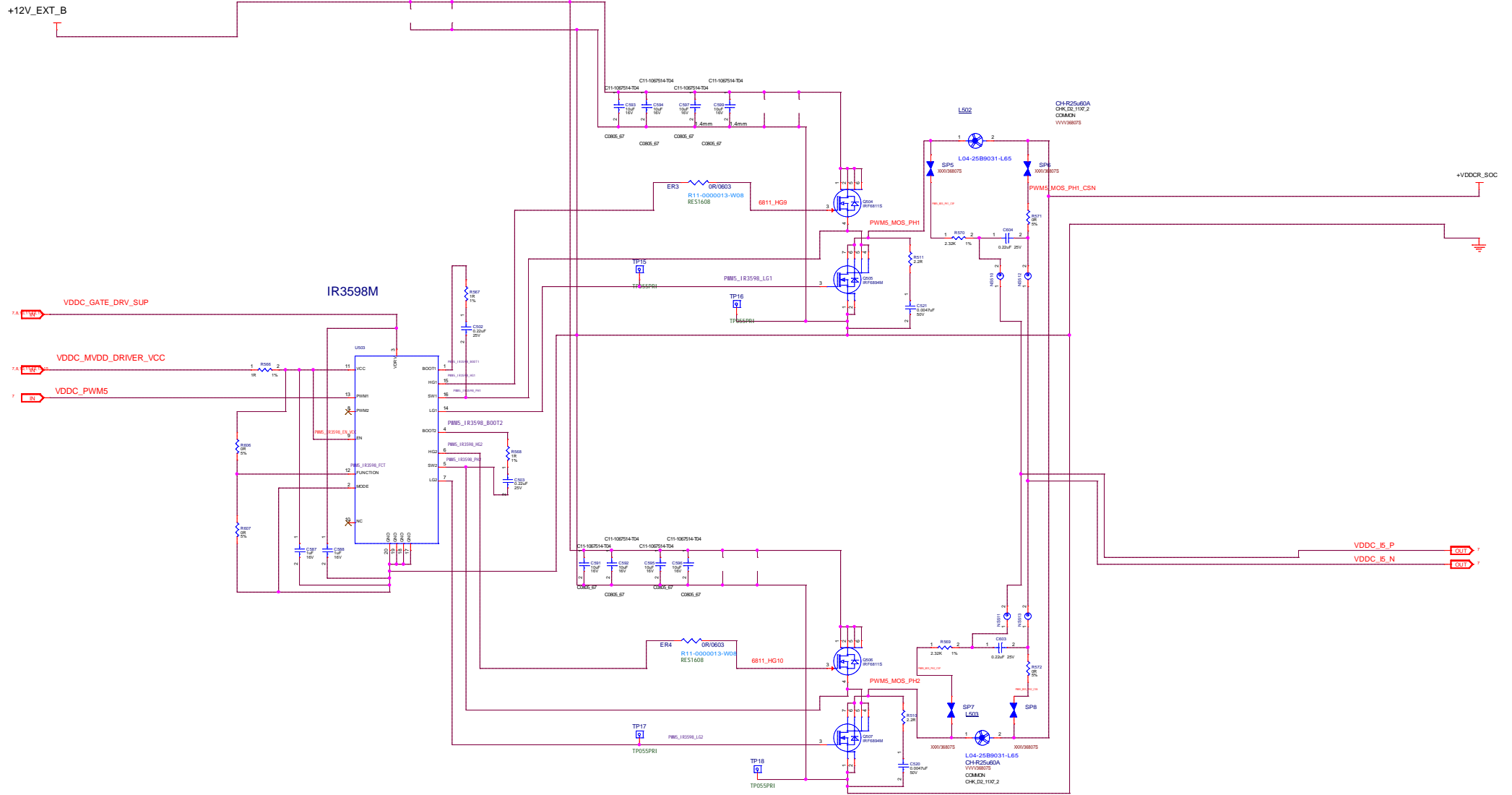
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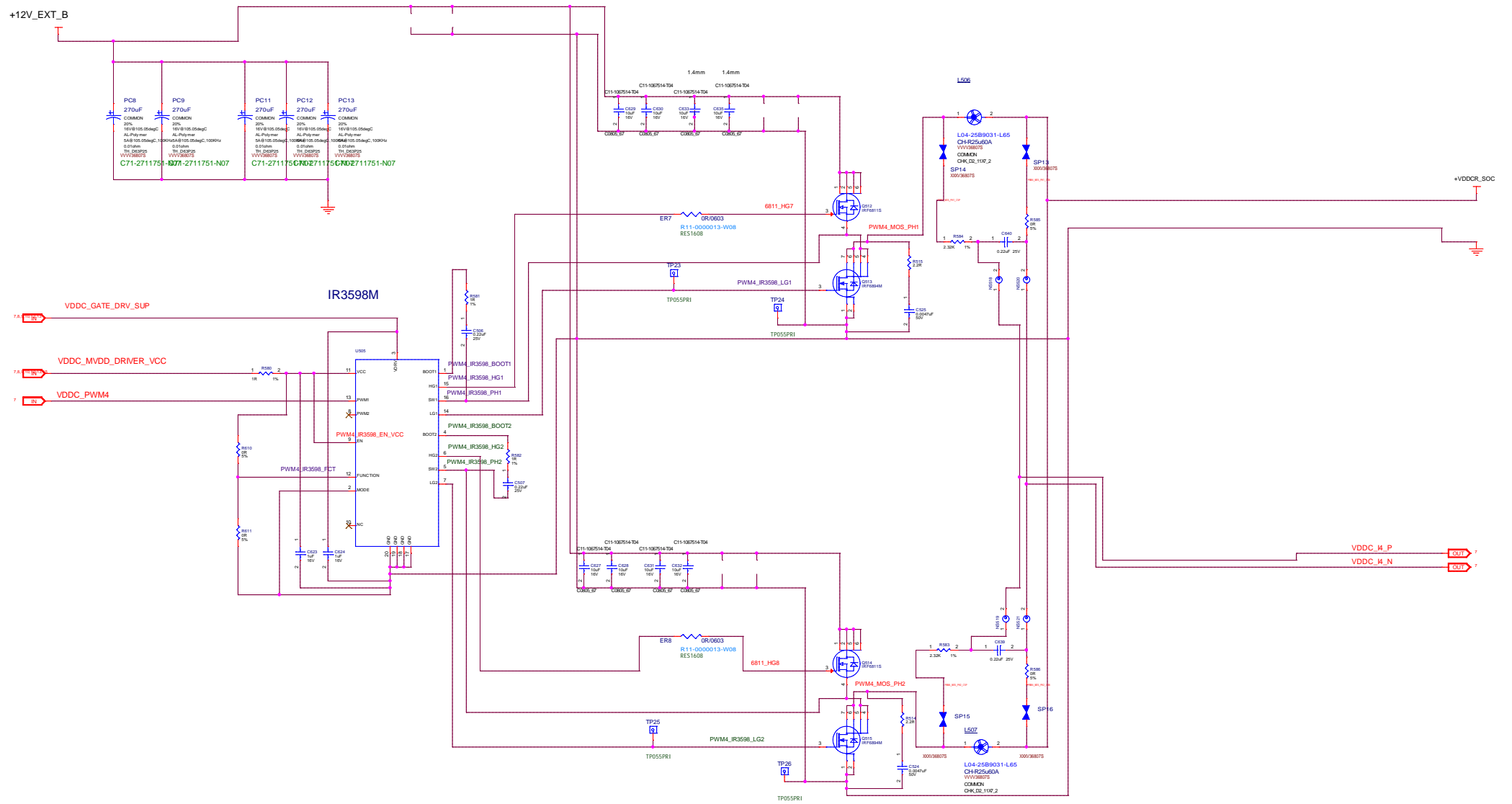


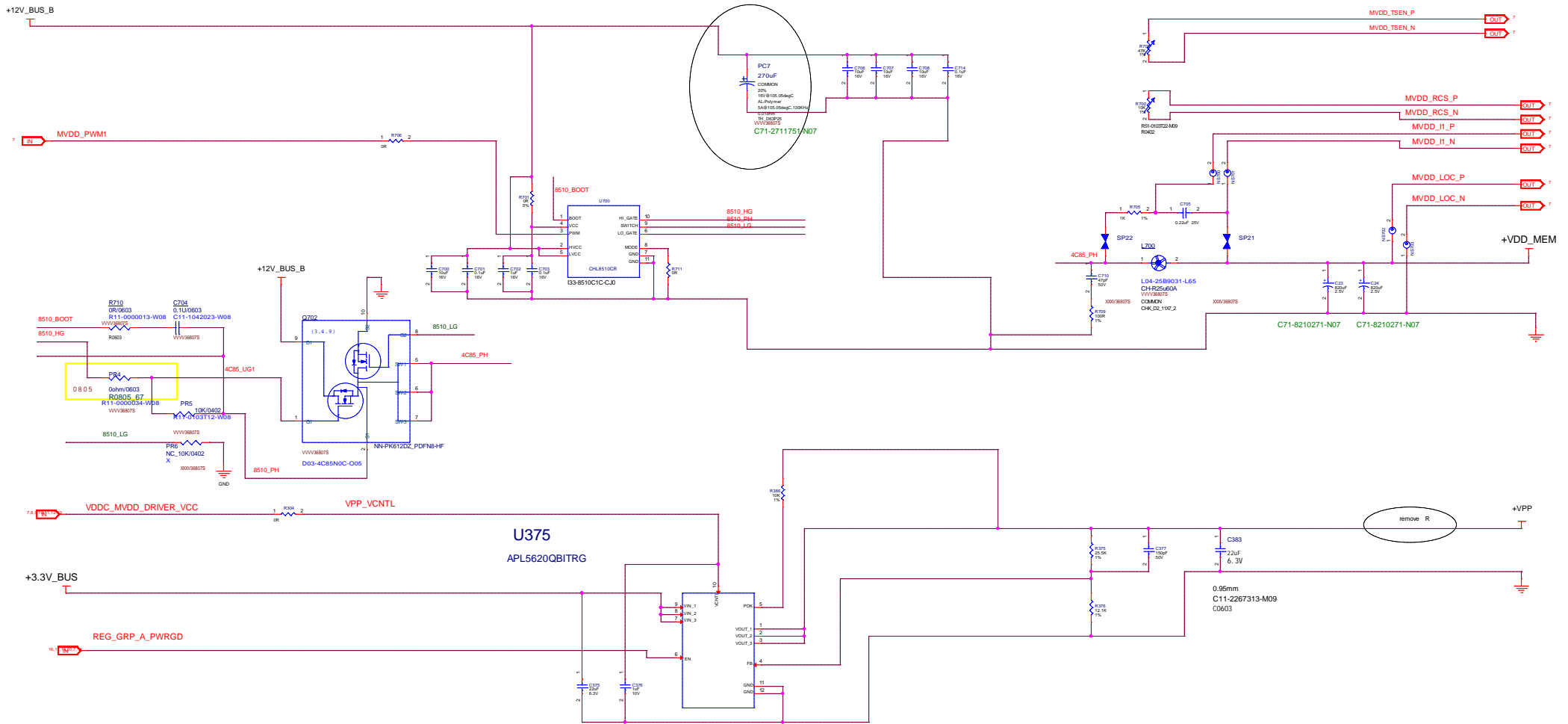
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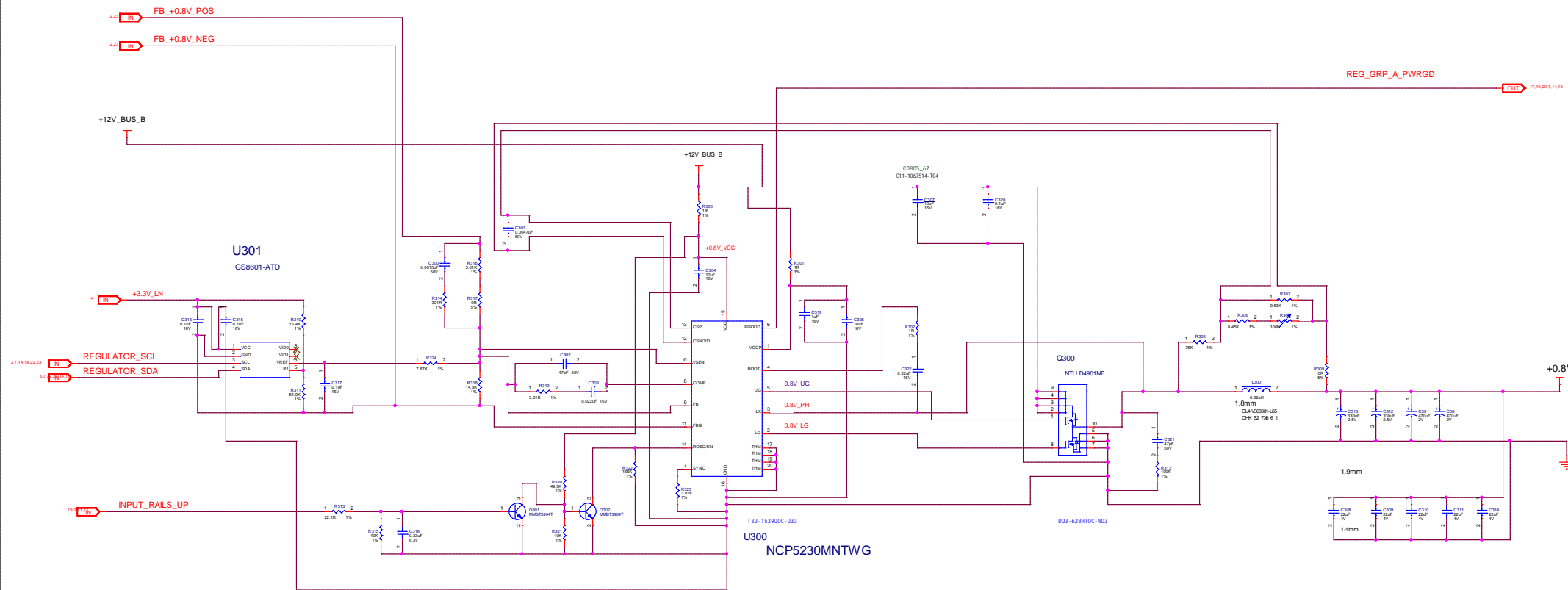
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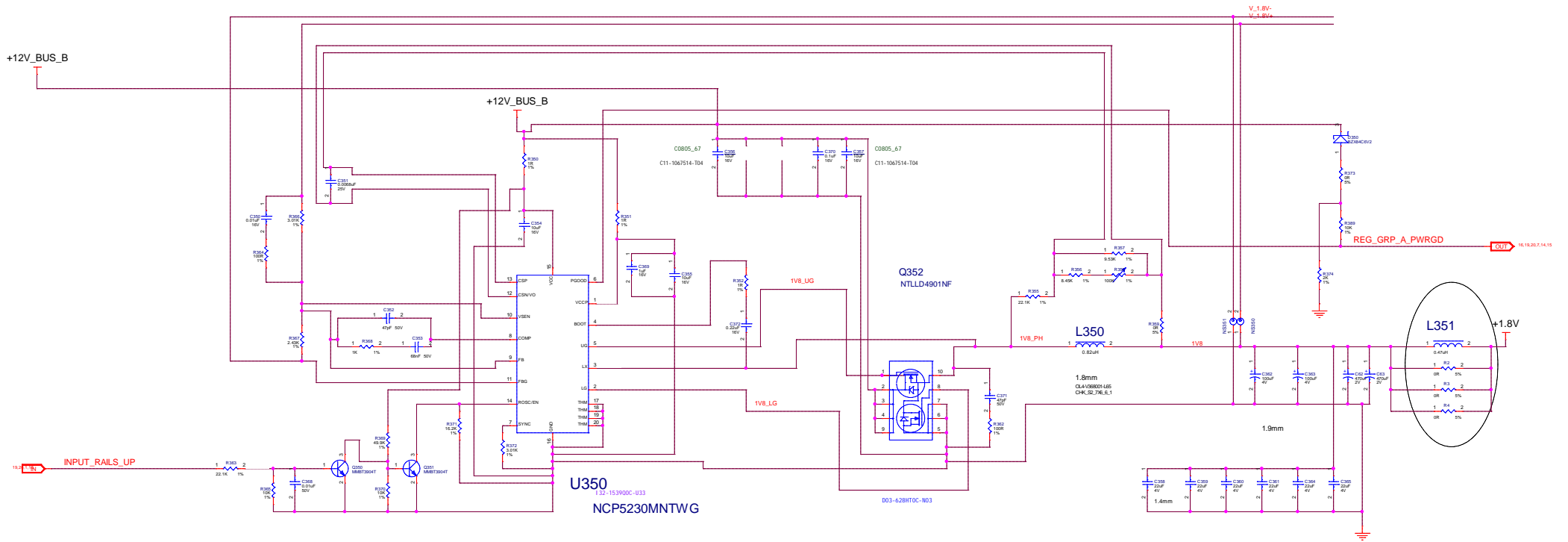
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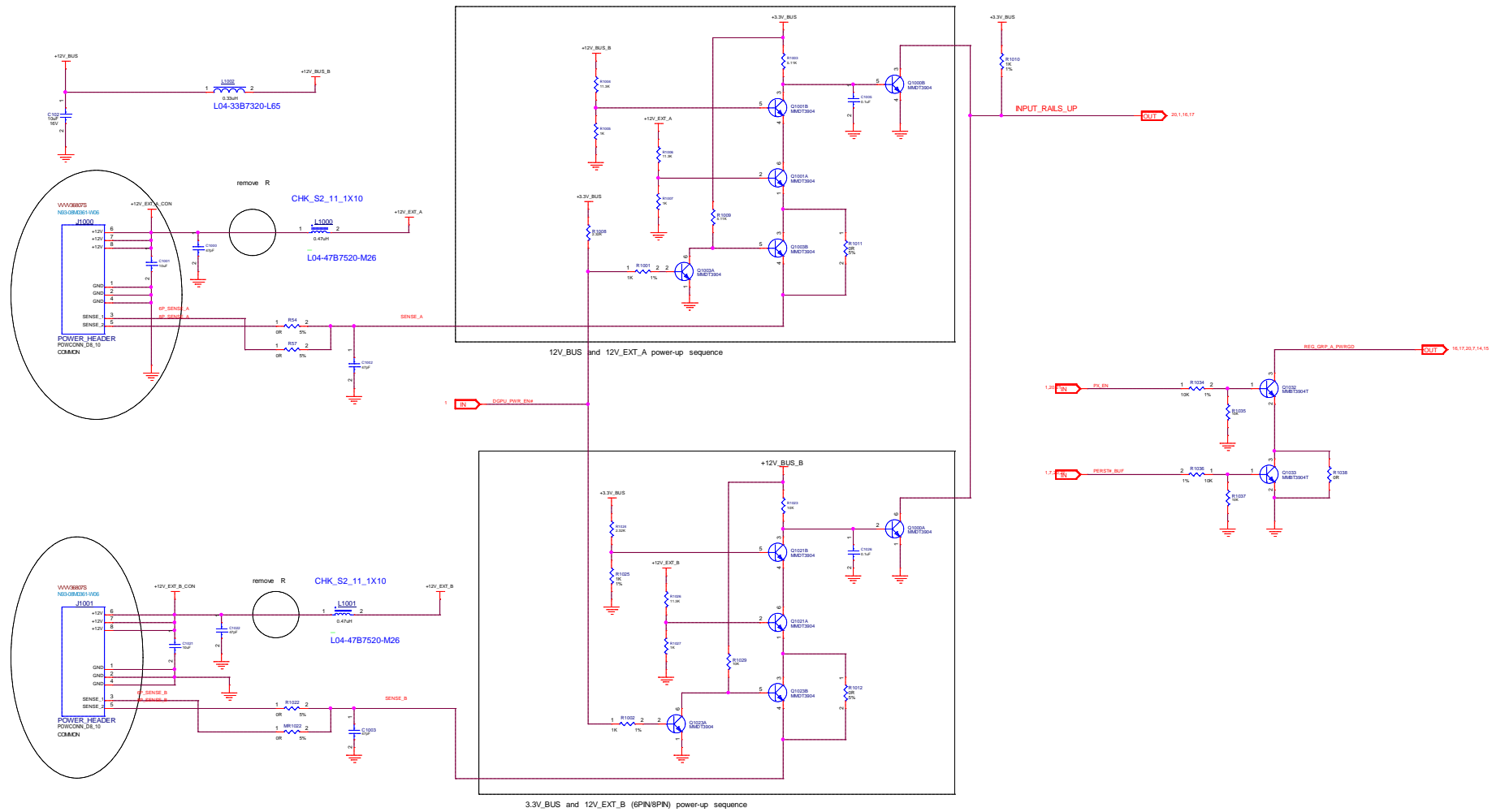


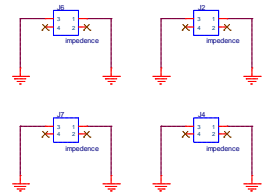
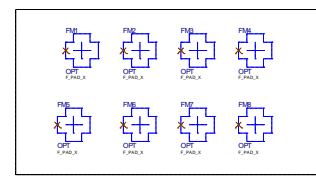
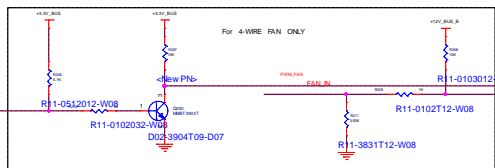
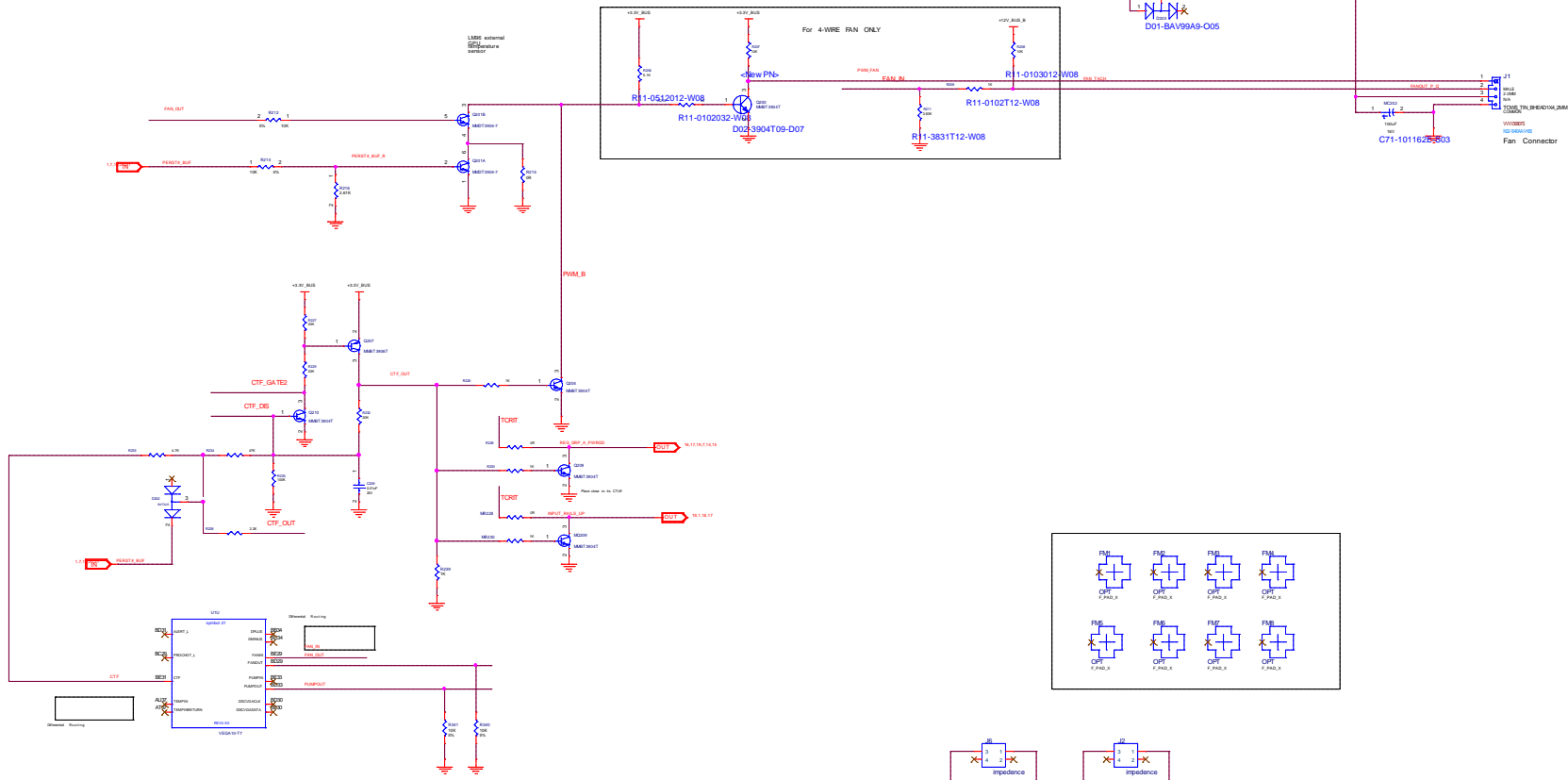
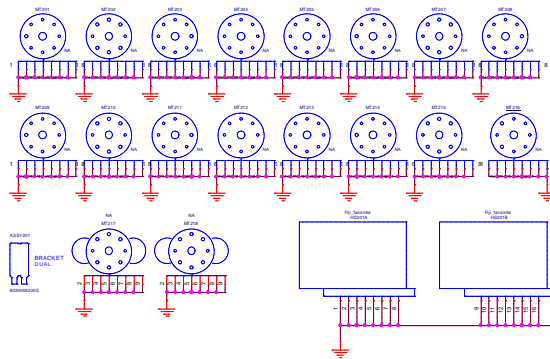




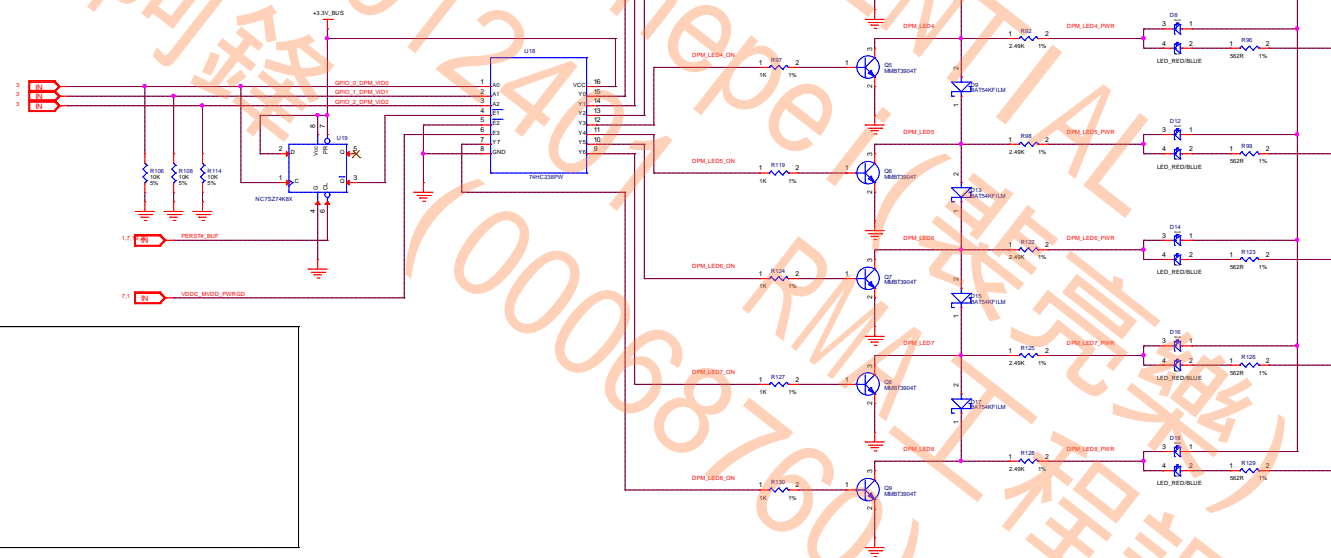
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LED GREEN "ON" indicates BACO mode



RADEON Lightbar header

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RD(C)2018012401 RMA工程課
石阿鋒 (00068760)

0	A	10/9/15	Initial schematic creation
B	6/30/16	Many Changes on PI circuit , Minor Chnages on SMPS	
C	9/30/16	Many Changes on PI circuit , ASIC SYMBOL UPDATED FOR FLASH ROM INTERFACE , flash ROM Si/So swapped , RP1 added	
D	11/29/16	Changes on PI circuit , 100MHz HCSSL clock source replced (contact AMD for detailes)	
E	01/05/17	PI circuit removed , 200R added to DP AUX (6 resistors)	
-00	02/02/17	1.8V/VPP Kelvin resistors dual footprinted , DP AUX (6 resistors changed to 100R) , Changed R4033 to 360R 1206 and moved to 12V_AUX , SMBUS Address note swap , J4001 removed , R115/R116 changed to 61.9R , R205 added	

